Scalability of the graphene/semiconductor barristor targeting digital applications

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Abstract

We have investigated the electrostatics and current-voltage characteristics of the graphene/semiconductor barristor [1] (see Fig. 1) considering effects of Fermi-level pinning (FLP) arising by possible presence of surface states, similarly to the metal-semiconductor junction [2]. Our study suggests that the barristor is a graphene logic device achieving high on/off current ratio, potentially of great interest for switching applications. When FLP dominates, the barristor's electrostatics the gate electrode cannot modulate the Schottky barrier height (SBH) and rectification could be totally lost [3]. On the other hand, our model has revealed that the Barristor exhibits changes of the threshold voltage by the source-drain voltage, similar to the Drain Inducend Barrier Lowering in conventional short channel MOSFETs. It turns out that the barristor has to be biased at low Vds to get a sufficient ON-OFF current ratio. As a final note, we have investigated the impact that a non-ideal interface might have in the barristor operation, and we have pointed out the role of oxide thickness scaling could have to get appropiate digital performance (Fig. 2).

References

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Figures

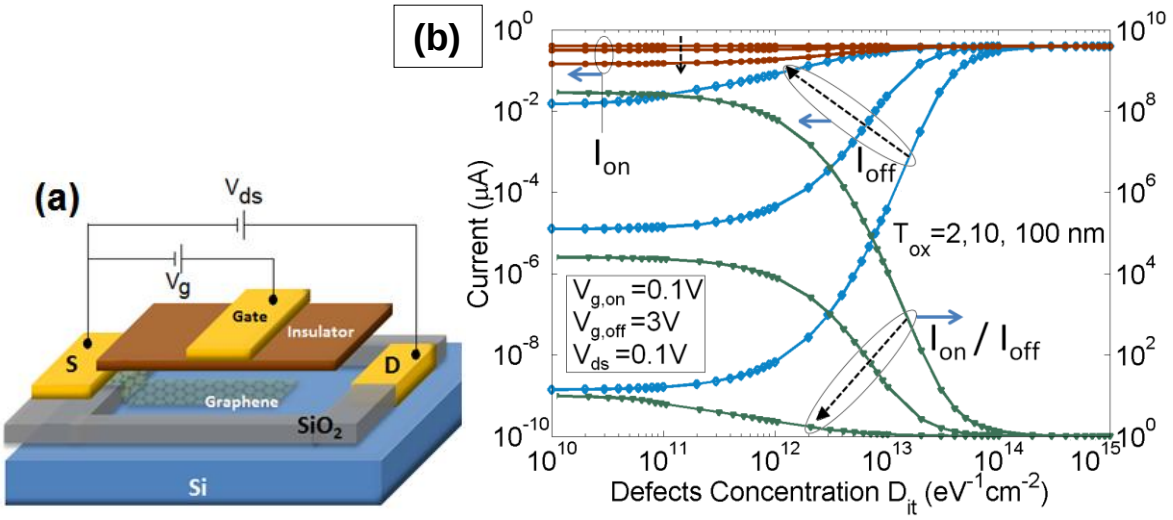

Figure 1. (a) Skecht of the barristor device, (b) Figures of merit of the barristor for different oxide thickness as a function of defects concentration at the graphene/semiconductor interface.